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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,485	09/10/2003	**Lakshman S. Tamil**	27592-00373	3440

30678 7590 05/29/2008

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EXAMINER	
PASCAL, LESLIE C	
ART UNIT	**PAPER NUMBER**
2613	

MAIL DATE	DELIVERY MODE
05/29/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/659,485	TAMIL, LAKSHMAN S.	
	Examiner	Art Unit	
	Leslie Pascal	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3-10-08*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62 and 68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-62 68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 8-10, 22-28, 31-40, 43-44, 46-48, 50-54, 57-62 and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jagannathan (6763192).

Jagannathan teaches an optical matrix switch (525) which inherently has plural inputs and plural outputs. It is well known that a switch matrix has intersections of the input and output links (i.e. matrix). He teaches that it is well known to use SOAs as the switching elements in an optical switch matrix (column 1, lines 29-37). It would have been obvious to use SOAs as the switching elements in the switching matrix of elements 525 since they switch extremely fast (at nano second response range) and are able to act as synchronous or asynchronous fixed or variable length packet switching apparatus (column 1, lines 32-37). In regard to the time interval, see column 4, lines 15-21. In regard to avoiding contention, see column 4, lines 47-55. It is obvious that the mapping and instructions of how to route the signals and how long the switches are to remain open are used to avoid contention problems. In regard to claim 4, see column 4, lines 47-55 in which he talks about the time interval. In regard to claim 5, see claim 16 of Jagannathan. He teaches switching plural wavelengths from one input to an output. It would appear that the signal would have to be multiplexed in some way in order to be switched from the input to the output. Jagannathan teaches a packet scheduler (405, 505, 520), a switch controller (410) which provides control of the switch (525). He teaches that there is DETAILED mapping used by the switch controller that can be proved by software computer program or hardware devices (column 4, lines 40-51). It is obvious that a computer program that provides the detailed mapping would be concerned with contention and capacity of the system in order to avoid lost signals which would occur if there was overloading and contention. In regard to claim 10, Jagannathan teach that the signal can be sent to a single output. In regard to the cross bar switch of claim 22, it would appear that by using an IXN or NXI SOA, such a crossbar would be made. The applicant's disclosure appears to teach that such elements are well known. So, it appears that would have been obvious in view of Jagannathan since he teaches that it is well known to use SOAs. In regard to claims 40 and 28, it would appear inherent that elements with "sufficient bandwidth" would work in the system or the system would not operate correctly. In regard to claim 45, Jagannathan teach that it is well known to have plural ingress (105) and egress Edge units connected to switch node devices (see figure 1). It would have been obvious to have plural edge units as taught by the prior art in order to provide proper connections from the edge units and switching devices since Jagannathan teach that it is well

known. In regard to claims 9 and 47-48, it would have been obvious to combine information that is going to the same egress node (or output) together as a multiplexed signal in order to ensure that signals destined for the same egress node (output node) all make it to the egress node without collision with others or each other.

3. Claims 11-12, 14-16, 19-21, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jagannathan (6763192) in view of Shiragaki et al (5757526)

Although Jagannathan (6763192) do not specifically teach that his switch matrix is made up of plural switching elements, Shiragaki et al teaches that it is well known (FIGURE 10) to use a switching matrix which is made up of plural matrix elements connected to each other (figure 10). It would have been obvious to use an array of matrix as taught by Shiragaki as the matrix switch of Jagannathan (6763192). It would have been obvious to use SOAs in the switching elements as taught by Jagannathan as well known in the prior art.

4. Claims 11-12 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robissa et al (2002/0163693).
Robissa et al teach plural switch matrices (figures 22-35, specifically figure 26) which have plurality of inputs (inputs), plural outputs (outputs), and plural path switches with specific path switch elements (402) a plurality of cross links (see specifically figures 26-29). With regard to the cross links, see paragraph 100 of Robissa et al in which he teaches that the connections may be fibers (links). It would have been obvious, if not inherent, to use links between the matrix in order to provide proper alignment between the switch matrix elements. In regard to claim 15, it would have been obvious to have just one input communicate with just one output, if the signal is only intended for one output. See paragraph 341 in which he teaches that the amount that the switch element is activated controls which percentage of the signal is sent to the intended switch.

5. Claims 13 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robissa et al (2002/0163693) as applied to claims 11-12 and 14-16 and further in view of Jagannathan (6763192) or in the alternative Jagannathan in view of Robissa. Although Robissa et al do not teach specifics about the type of switch elements used, it would have been obvious to use the SOAs taught by Jagannathan as the switch elements of Robissa et al. In the alternative, it would have been obvious to use Jagannathan in view of Robissa by replacing the switch matrix specifics of Jagannathan with the 3d switch matrix of Robissa et al since Robissa teaches that his system could be used 2D as taught by Jagannathan or 3D. Jagannathan teaches that packet scheduler and switch controller of claims 19-21

6. Claims 6-7, 29-30, 41-42 and 55-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jagannathan and further in view of Antoniades et al (2002/0048066).

Although Jagannathan does not teach specifics about the conditioning means at the input and output of the switch, Antoniades et al teaches that it is well known to the input and output in order to provide stronger signals and that it is obvious to filter them (paragraph 80). It would have been obvious to amplify the inputs and outputs in order to provide a stronger signals and it would have been obvious to filter the signals in order to reduce ripple.

7. Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robissa as applied to claims 11-12 in view of Antoniades et al (200210048066). Although Robissa does not teach specifics about the conditioning means at the input and output of the switch, Antoniades et al teaches that it is well known to amply signals at the input and output in order to provide stronger signals and that it is obvious to filter them (paragraph 80). It would have been obvious to amplify the inputs and outputs in order to provide a stronger signals and it would have been obvious to filter the signals in order to reduce ripple.

8. Applicant's arguments filed 3-10-08 have been fully considered but they are not persuasive. The applicant has amended the claims to include a switch controller to ensure that capacity of the plurality of the output links is not exceeded and a packet scheduler to receive and process a plurality of control packet data links. The previous action addressed a switch controller and packet scheduler which were claimed in dependent claims. The reference teaches a switch controller (410) and a packet scheduler (405, 505, 520). He teaches that there is DETAILED mapping used by the switch controller that can be proved by software computer program or hardware devices (column 4, lines 40-51). It is obvious that a computer program that provides the detailed mapping would be concerned with contention and capacity of the system in order to avoid lost signals which would occur if there was overloading and contention.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leslie Pascal whose telephone number is 571-272-3032. The examiner can normally be reached on Monday- Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leslie Pascal/
Primary Examiner
Art Unit 2613